What is claimed is:

[Claim 1] 1. A thin film transistor array semi-finished product structure over a substrate having at least one designated display region, comprising:

a first patterned conductive layer over the substrate, wherein the first patterned conductive layer distributes over an area range that exceeds the designated display region;

a dielectric layer covering a portion of the first patterned conductive layer but exposing the first patterned conductive layer outside the designated display region; and

a second patterned conductive layer over the dielectric layer, wherein the second patterned conductive layer and the exposed first patterned conductive layer are electrically connected.

[Claim 2] 2. The structure of claim 1, wherein the first patterned conductive layer includes a plurality of gates and a plurality of gate connected scan lines.

[Claim 3] 3. The structure of claim 1, wherein material constituting the first patterned conductive layer includes a metallic substance.

[Claim 4] 4. The structure of claim 3, wherein material constituting the first patterned conductive layer is selected from a group consisting of chromium and tantalum.

[Claim 5] 5. The structure of claim 1, wherein material constituting the dielectric layer includes silicon nitride.

[Claim 6] 6. The structure of claim 1, wherein material constituting the second patterned conductive layer includes a metallic substance.

[Claim 7] 7. The structure of claim 6, wherein material constituting the second patterned conductive layer includes aluminum.